REMARKS

Claims 1-3, 5 and 10 are amended. No new subject matter is added.

Claim rejections - 35 USC § 102

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,862,096 to Yasuda, et al. ("Yasuda"). The applicant disagrees.

Claims 1-3 and 5 are amended to remove unnecessary wordage. No new subject matter is added.

In order to anticipate a claim, the ***identical invention*** must be shown in as complete detail as contained in the claim. MPEP 2131, emphasis added.

Independent claim 1 recites, *inter alia*, a memory cell array that includes memory cell array blocks arranged in the column direction. It is alleged that Yasuda discloses memory cell array blocks 4a-4d (FIG. 1). To the contrary, Yasuda (FIG. 1) illustrates that 4a, 4b, 4c, 4d are defined as memory cell arrays, not memory cell array blocks. Thus, while Yasuda does show memory cell arrays 4a-4d, Yasuda contains no teaching that any one of the memory cell arrays 4a-4d includes memory cell array blocks arranged in the column direction.

Claim 1 also recites a column decoder arranged on a first side of the memory cell array and configured to select one of the column selecting lines.

If, as is suggested, the entire structure of Yasuda's FIG. 1 is the recited memory cell array, then FIG. 1 shows that none of the column related control circuits 5a, 5b, 5c, 5d are arranged on a first side of the memory cell array. In this case, the column related control circuits 5a-5d are clearly not arranged on a first side of the memory cell array.

If Yasuda teaches, and the applicant submits that it does, that there are four memory cell arrays 4a-4d illustrated in FIG. 1, then the column related control circuits 5a-5d may be said to be arranged to a first side of their respective memory cell arrays 4a-4d (FIG. 1).

However, claim 1 also recites an internal voltage generating circuit arranged on both the first and a second side of the memory cell array. Yasuda FIG. 1 shows that if column-related control circuits 5a-5d are arranged on a first side of their respective memory cell arrays 4a-4d, then none of the circuits 10, 11, 12a, and 12b are arranged on ***both*** the first side and a second side of their respective memory cell arrays 4a-4d (emphasis added).

Claim 1 also recites internal voltage generating lines arranged between the memory cell array blocks. Yasuda FIG. 1 shows that while there may be internal voltage generating lines arranged between the memory cell arrays 4a-4d, it certainly does not indicate that

internal voltage generating lines are arranged between memory cell array blocks that are included in the memory cell arrays 4a-4d.

Claim 1 further recites drivers arranged on both ends of the internal voltage generating lines. Yasuda contains no teaching that indicates the alleged drivers (apparently the driver transistors 10bb, 25c of FIGs. 2 and 3) are arranged on both ends of the alleged internal voltage generating lines (internal power supply lines 20/20a).

For any one of the above reasons, Yasuda does not anticipate claim 1 for failing to show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claims 2-5 depend from claim 1, and inherently contain the features of claim 1. Consequently, Yasuda also fails to anticipate claims 2-5 at least because it does not show the identical invention in as complete detail as is inherently contained in the claim. MPEP 2131.

Independent claim 6 recites, *inter alia*, a first and a second driver coupled to the first and the second active internal voltage generating circuits, respectively, and coupled to a first and a second end, respectively, of the internal voltage generating line.

Yasuda contains no teaching that indicates the alleged first and a second drivers (apparently the driver transistors 10bb, 25c of FIGs. 2 and 3) are coupled to a first and second end, respectively, of the alleged internal voltage generating line (internal power supply lines 20/20a).

For at least the reason presented above, Yasuda does not anticipate claim 6 because it fails to show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claims 7-8 depend from claim 6, and inherently contain the features of claim 6. Consequently, Yasuda also fails to anticipate claims 7-8 at least because it does not show the identical invention in as complete detail as is inherently contained in the claim. MPEP 2131.

Claims 10 is amended to remove unnecessary wordage. No new subject matter is added.

Independent claim 9 recites, *inter alia*, arranging drivers of the active internal voltage generating circuit on two sides of the internal voltage generating lines.

Yasuda contains no teaching that indicates the alleged drivers of the active internal voltage generating circuit (apparently the driver transistor 25c of FIG. 3) is arranged on two sides of the alleged internal voltage generating lines (internal power supply lines 20/20a).

For at least the reason presented above, Yasuda does not anticipate claim 9 because it fails to show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claims 10-11 depend from claim 9, and inherently contain the features of claim 9. Consequently, Yasuda fails to anticipate claims 10-11 at least because it does not show the identical invention in as complete detail as is inherently contained in the claim. MPEP 2131.

Additionally, claim 10 recites arranging first drivers of the active internal voltage generating circuit on one side of the internal voltage generating lines and arranging second drivers of the active internal voltage generating circuit on another side of the internal voltage generating lines.

Yasuda contains no teaching that indicates the alleged first drivers (apparently the driver transistor 25c of FIG. 3) is arranged on one side of the internal voltage generating lines (internal power supply line 20/20a) ***and*** the alleged second drivers (apparently the driver transistor 25c of FIG. 3) is arranged on another side of the internal voltage generating lines (emphasis added).

Independent claim 12 is directed at a method that includes, *inter alia*, coupling a first driver from a first active internal voltage circuit to a first end of an internal voltage generating line, and coupling a second driver from a second active internal voltage circuit to a second end of the internal voltage generating line.

Yasuda contains no teaching that indicates the alleged first driver (apparently the driver transistor 10bb, 25c of FIGs. 2 and 3) is coupled to a first end of an internal voltage generating line (internal power supply line 20/20a) ***and*** the alleged second driver (apparently the driver transistor 10bb, 25c of FIGs. 2 and 3) is coupled to a second end of the same internal voltage generating line (emphasis added).

For at least the reason presented above, Yasuda does not anticipate claim 12 because it fails to show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claims 13-15 depend from claim 12, and inherently contain the features of claim 12. Consequently, Yasuda also fails to anticipate claims 13-15 at least because it does not show the identical invention in as complete detail as is inherently contained in the claim. MPEP 2131.

Additionally, claim 15 recites that coupling the first driver and coupling the second driver includes arranging the first driver and the second driver between two column selecting lines.

Yasuda contains no teaching that the alleged first and second drivers (apparently the driver transistor 25c of FIG. 3) are arranged between two column selecting lines. Consequently, for this additional reason Yasuda fails to anticipate claim 15 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Conclusion

For the above reasons, reconsideration and allowance of claims 1-15 is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Todd J. Iverson
Reg. No. 53,057

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613
Customer No. 20575

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Li Mei Vermilya